30V Dual N-Channel MOSFETs

PDEB38G2BH

General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

	BVDSS	RDSON	ID
Q1	30V	6.8mΩ	40A
Q2	30V	6.8mΩ	40A

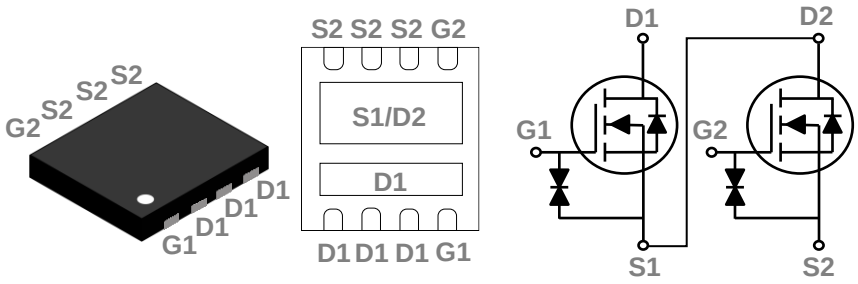
Features

- *Improved dv/dt capability*
- *Fast switching*
- *100% EAS Guaranteed*
- *Green Device Available*
- *ESD Protection Embedded*

Applications

- *MB / VGA / Vcore*
- *POL Buck Applications*
- *SMPS 2nd SR*

DFN3x3 Asymmetric Dual Pin Configuration



Absolute Maximum Ratings Tc=25℃ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D	Drain Current – Continuous (T_C=25℃)	40	40	A
	Drain Current – Continuous (T_C=100℃)	25	25	A
	Drain Current – Continuous (T_A=25℃)	13	13	A
	Drain Current – Continuous (T_A=100℃)	8	8	A
I_{DM}	Drain Current – Pulsed[1]	160	160	A
EAS	Single Pulse Avalanche Energy[2]	45	45	mJ
IAS	Single Pulse Avalanche Current[2]	30	30	A
P_D	Power Dissipation (T_C=25℃)	18	18	W
	Power Dissipation – Derate above 25℃	0.15	0.15	W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Characteristics

Symbol		Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Q1	Thermal Resistance Junction to ambient	---	62	℃/W
$R_{\theta JA}$	Q2		---	62	℃/W
$R_{\theta JC}$	Q1	Thermal Resistance Junction to Case	---	6.9	℃/W
$R_{\theta JC}$	Q2		---	6.9	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Static State Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250μA	Q1	30	---	---	V
			Q2	30	---	---	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=27V , V_{GS}=0V , T_J=25℃	Q1	---	---	1	μA
			Q2	---	---	1	μA
		V_{DS}=24V , V_{GS}=0V , T_J=85℃	Q1	---	---	10	μA
			Q2	---	---	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	Q1	---	---	±20	μA
			Q2	---	---	±20	μA
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=15A	Q1	---	5.7	6.8	mΩ
		V_{GS}=10V , I_D=15A	Q2	---	5.7	6.8	mΩ
		V_{GS}=4.5V , I_D=10A	Q1	---	8.6	11.2	mΩ
		V_{GS}=4.5V , I_D=10A	Q2	---	8.6	11.2	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250μA	Q1	1.2	1.6	2.5	V
			Q2	1.2	1.6	2.5	V

Dynamic Characteristics[3]

Q_g	Total Gate Charge	V_{DS}=15V , V_{GS}=10V , I_D=20A	Q1	---	13	25	nC
			Q2	---	13	25	
		V_{DS}=15V , V_{GS}=4.5V , I_D=20A	Q1	---	6.3	12	
			Q2	---	6.3	12	
Q_{gs}	Gate-Source Charge		Q1	---	1.1	3	
			Q2	---	1.1	3	
Q_{gd}	Gate-Drain Charge		Q1	---	2.2	5	
			Q2	---	2.2	5	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=6Ω I_D=20A	Q1	---	2.5	5	ns
			Q2	---	2.5	5	
T_r	Rise Time		Q1	---	3	6	
			Q2	---	3	6	
$T_{d(off)}$	Turn-Off Delay Time		Q1	---	5	10	
			Q2	---	5	10	
T_f	Fall Time		Q1	---	8	16	
			Q2	---	8	16	

C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , F=1MHz	Q1	---	680	1400	pF
			Q2	---	680	1400	
C_{oss}	Output Capacitance		Q1	---	507	1000	
			Q2	---	507	1000	
C_{rss}	Reverse Transfer Capacitance		Q1	---	27	60	
			Q2	---	27	60	
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz	Q1	---	1.5	---	Ω
			Q2	---	1.5	---	

Drain-Source Diode Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	Q1	---	---	40	A
			Q2	---	---	40	A
I_{SM}	Pulsed Source Current		Q1	---	---	80	A
			Q2	---	---	80	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=1A , T_J=25℃	Q1	---	---	1	V
			Q2	---	---	1	V

Note :
1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V,V_{GS}=10V,L=0.1mH,Q1:I_{AS}=30A,Q2:I_{AS}=30A,R_G=25Ω,Starting T_J=25℃.
3. Essentially independent of operating temperature.

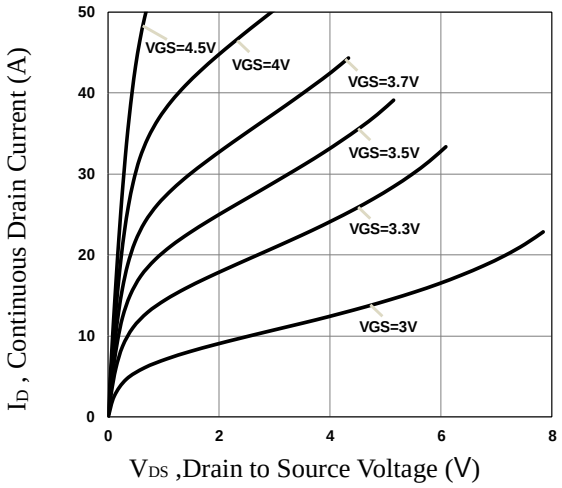


Fig.1 Q1 Typical Output Characteristics

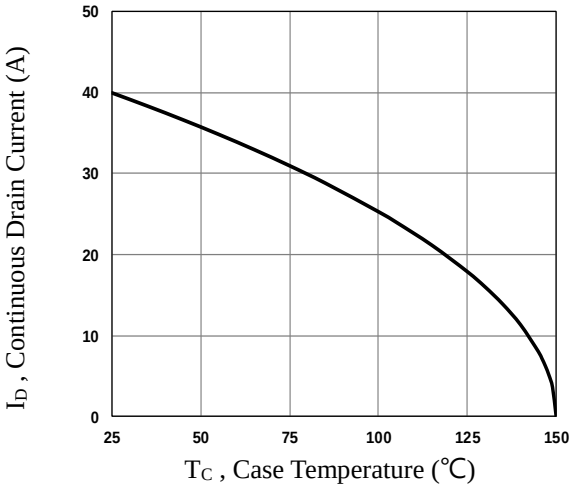


Fig.2 Q1 Continuous Drain Current vs. T_C

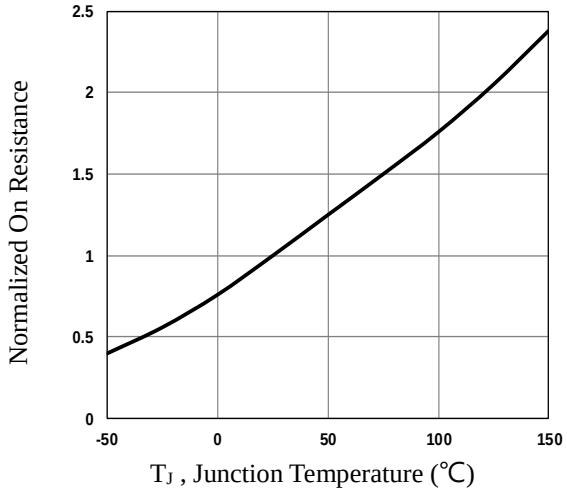


Fig.3 Q1 Normalized RDSON vs. T_J

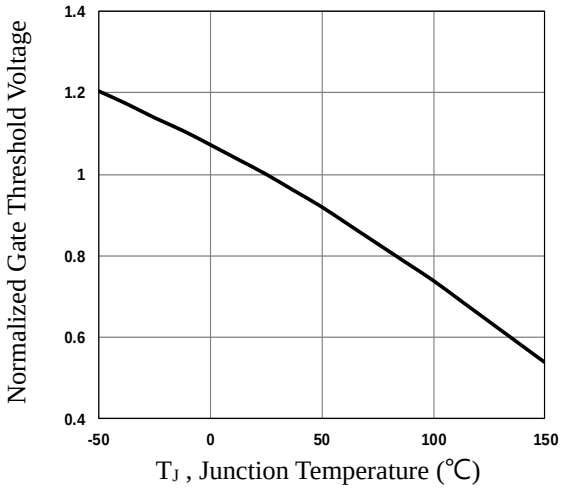


Fig.4 Q1 Normalized V_{th} vs. T_J

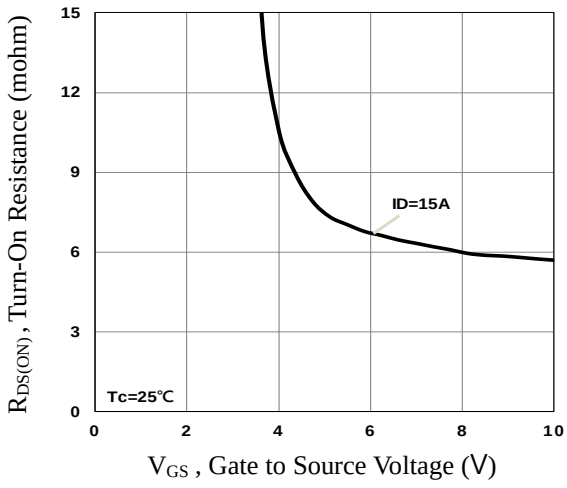


Fig.5 Q1 Turn-On Resistance vs. V_{GS}

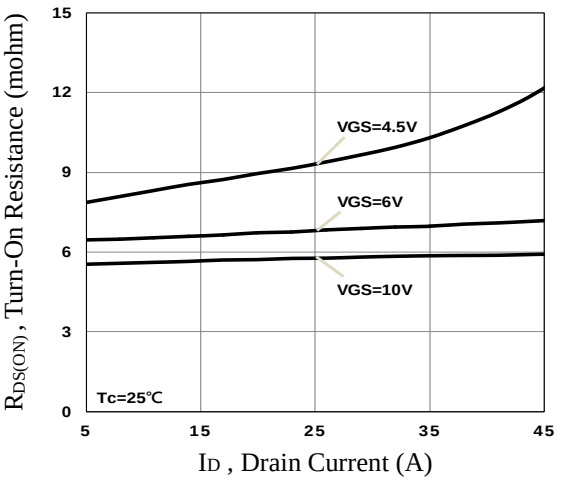


Fig.6 Q1 Turn-On Resistance vs. I_D

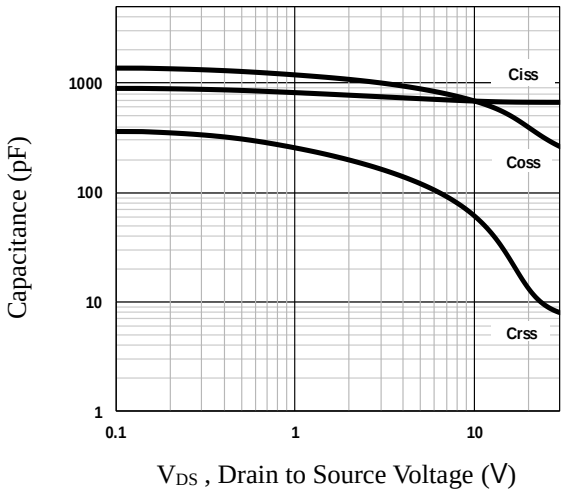


Fig.7 Q1 Capacitance Characteristics

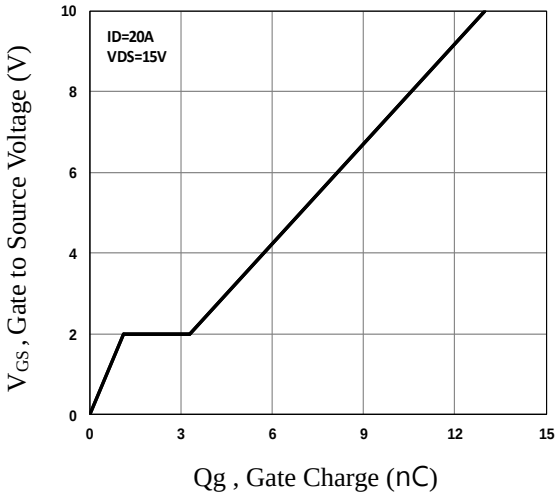


Fig.8 Q1 Gate Charge Characteristics

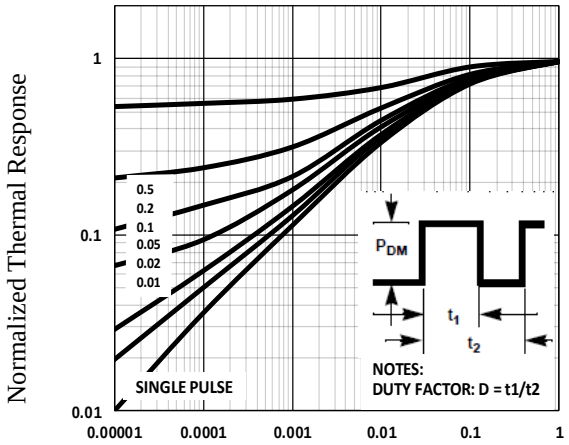


Fig.9 Q1 Normalized Transient Impedance

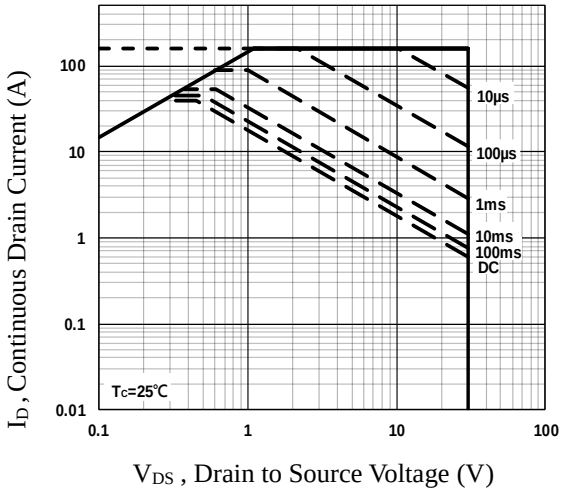


Fig.10 Q1 Maximum Safe Operation Area

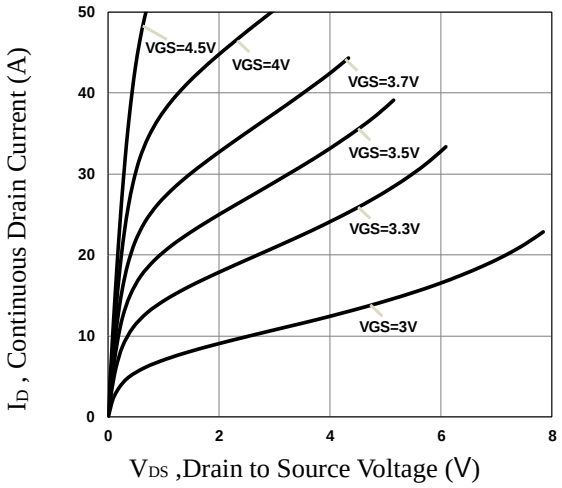


Fig.11 Q2 Typical Output Characteristics

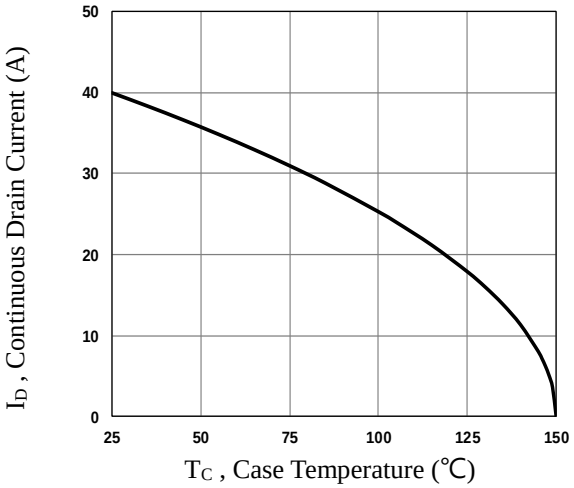


Fig.12 Q2 Continuous Drain Current vs. T_C

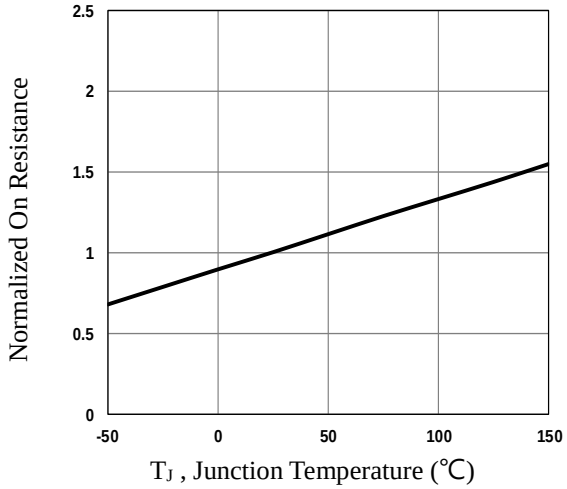


Fig.13 Q2 Normalized RDSON vs. T_J

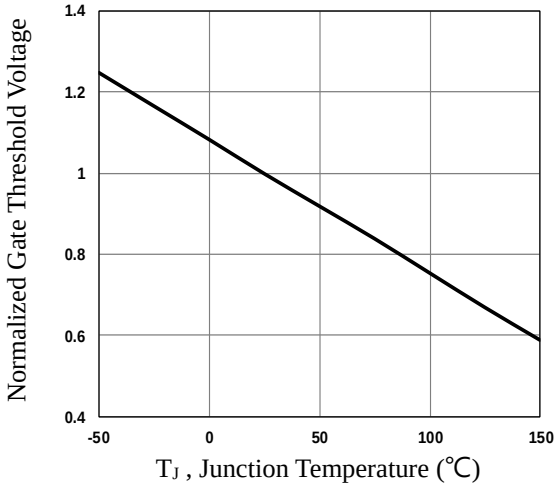


Fig.14 Q2 Normalized V_{th} vs. T_J

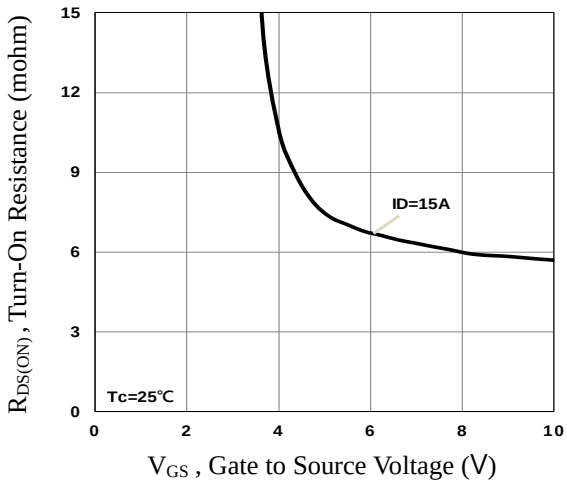


Fig.15 Q2 Turn-On Resistance vs. V_{GS}

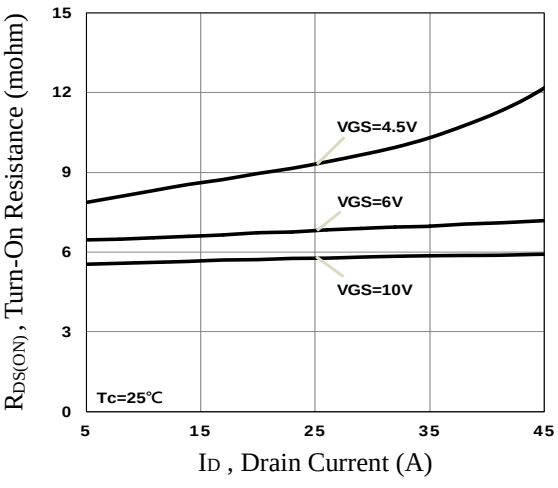


Fig.16 Q2 Turn-On Resistance vs. I_D

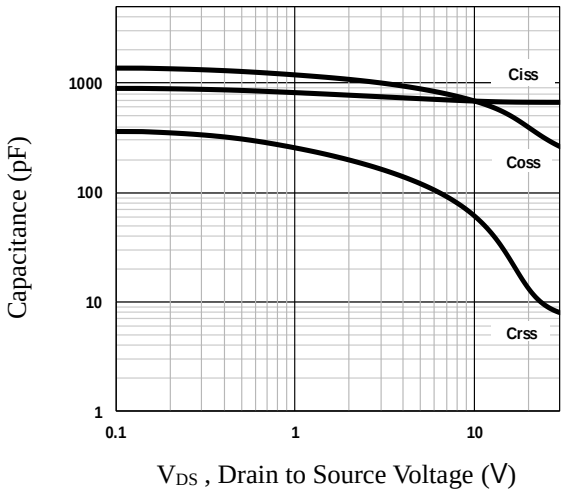


Fig.17 Q2 Capacitance Characteristics

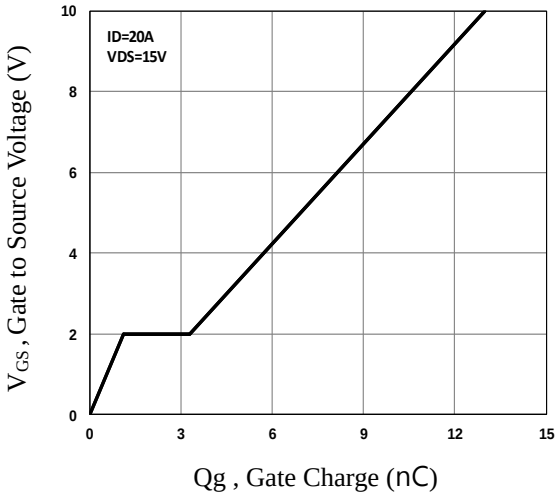


Fig.18 Q2 Gate Charge Characteristics

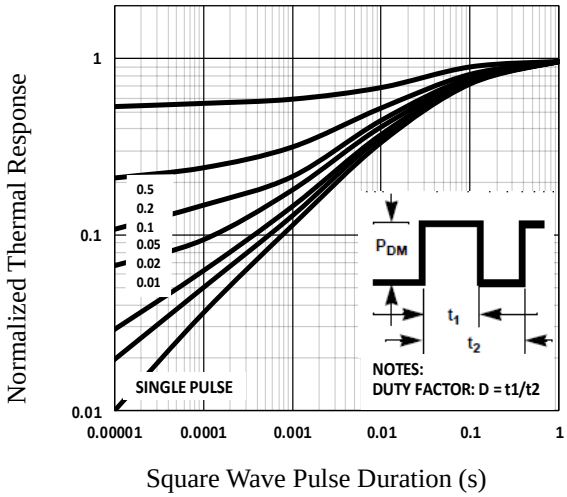


Fig.19 Q2 Normalized Transient Impedance

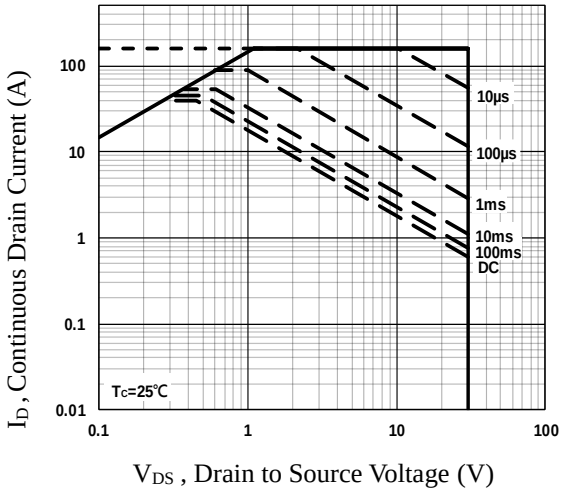


Fig.20 Q2 Maximum Safe Operation Area

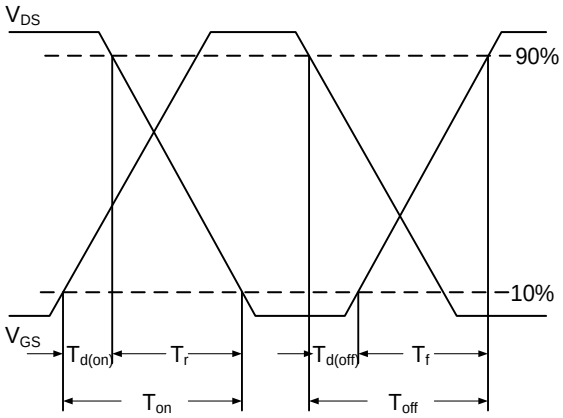


Fig.21 Switching Time Waveform

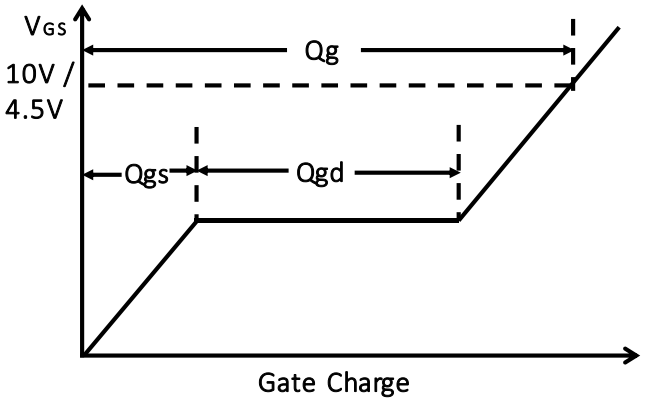
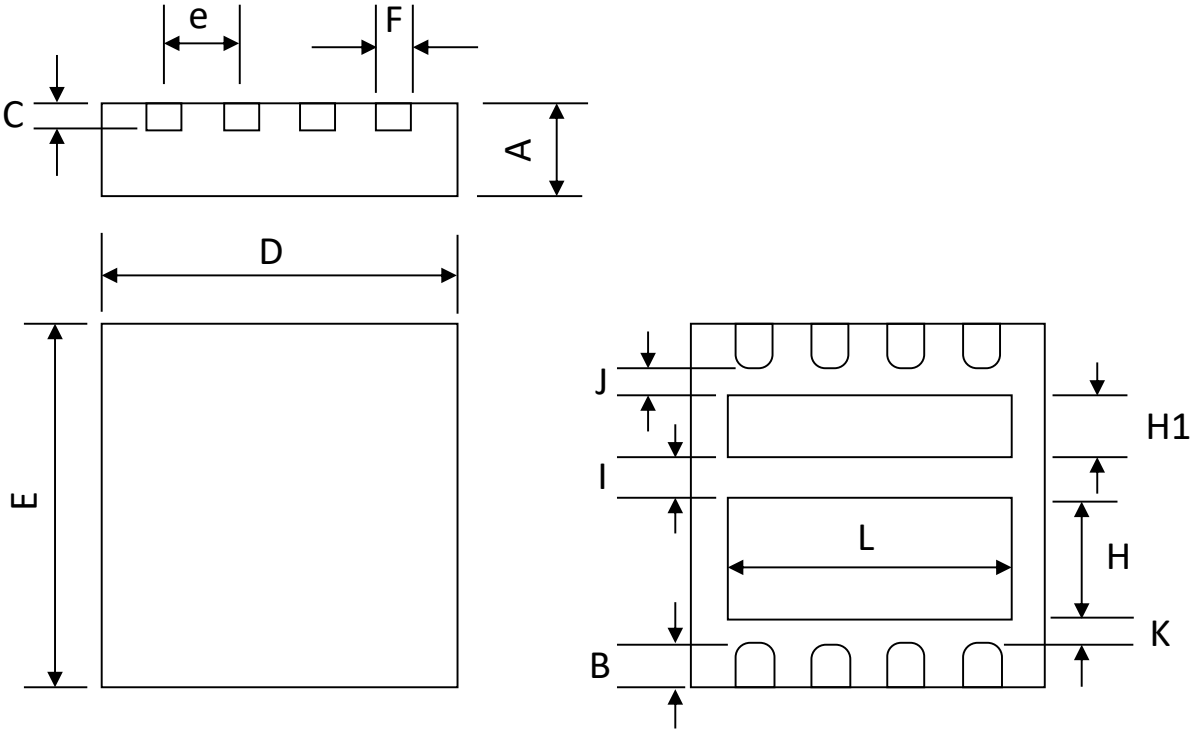


Fig.22 Gate Charge Waveform

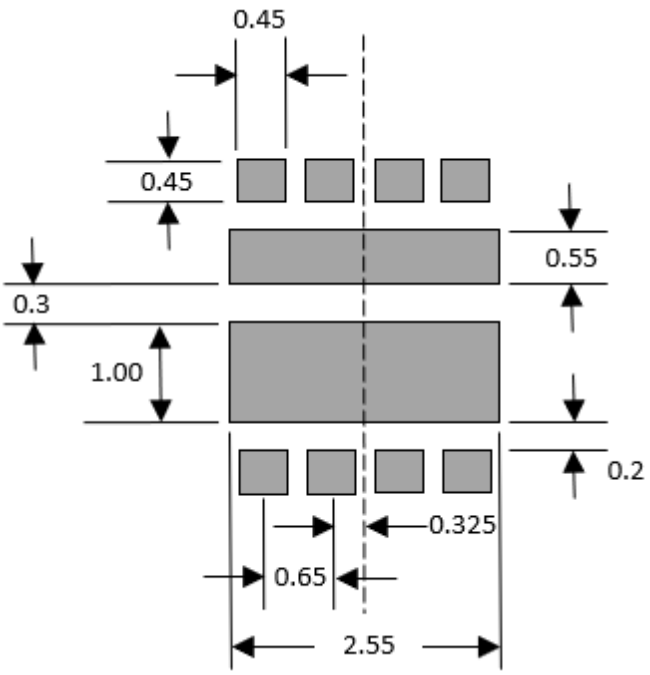
DFN3x3 Asymmetric Dual Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Max	Min	Max	Min
A	0.900	0.700	0.035	0.028
B	0.400	0.250	0.016	0.010
C	0.255	0.150	0.010	0.006
D	3.100	2.900	0.122	0.114
E	3.100	2.900	0.122	0.114
e	0.650 BSC		0.026 BSC	
F	0.450	0.250	0.018	0.010
H	1.100	0.850	0.043	0.033
H1	0.650	0.400	0.026	0.016
I	0.450	0.250	0.018	0.010
J	0.350	0.150	0.014	0.006
K	0.350	0.150	0.014	0.006
L	2.500	2.200	0.098	0.087

RECOMMENDED LAND PATTERN

DFN3X3 (Asymmetric Dual)



unit : mm