

### General Description

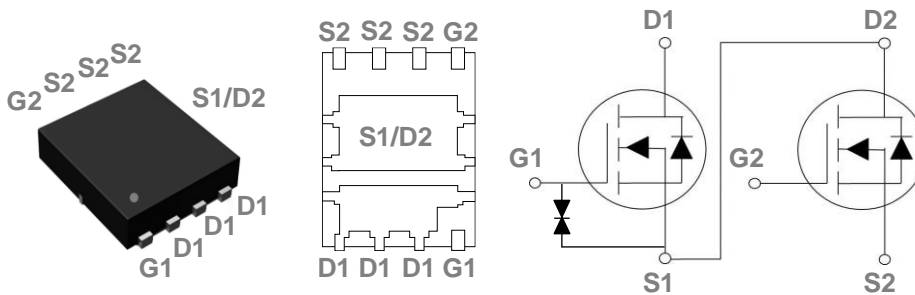
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

	BVDSS	RDSON	ID
Q1	30V	5mΩ	45A
Q2	30V	2.6mΩ	85A

### Features

- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available

### PPAK5x6 Asymmetric Dual Pin Configuration



### Applications

- MB / VGA / Vcore
- POL Buck Applications
- SMPS 2<sup>nd</sup> SR

### Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain-Source Voltage	30	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 12$	V
$I_D$	Drain Current – Continuous ( $T_c=25^\circ\text{C}$ )	45	85	A
	Drain Current – Continuous ( $T_c=100^\circ\text{C}$ )	28.5	54	A
$I_{DM}$	Drain Current – Pulsed <sup>1</sup>	180	340	A
EAS	Single Pulse Avalanche Energy <sup>2</sup>	60	140	mJ
IAS	Single Pulse Avalanche Current <sup>2</sup>	34.5	53	A
$P_D$	Power Dissipation ( $T_c=25^\circ\text{C}$ )	17.5	33	W
	Power Dissipation – Derate above $25^\circ\text{C}$	0.14	0.26	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$ Q1	Thermal Resistance Junction to ambient ( $t \leq 10\text{s}$ )	---	40	$^\circ\text{C/W}$
$R_{\theta JA}$ Q2		---	40	$^\circ\text{C/W}$
$R_{\theta JC}$ Q1	Thermal Resistance Junction to Case	---	7.1	$^\circ\text{C/W}$
$R_{\theta JC}$ Q2		---	3.8	$^\circ\text{C/W}$

**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**
**Static State Characteristics**

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	Q1	30	---	---	V
			Q2	30	---	---	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =27V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	Q1	---	---	1	μA
			Q2	---	---	1	μA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =85°C	Q1	---	---	10	μA
			Q2	---	---	10	μA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	Q1	---	---	±20	μA
		V <sub>GS</sub> =12V, V <sub>DS</sub> =0V	Q2	---	---	100	nA
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>3</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	Q1	---	4.2	5	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =20A	Q2	---	2.1	2.6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	Q1	---	6.4	8.3	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	Q2	---	2.5	2.95	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	Q1	1.2	1.7	2.5	V
			Q2	1.2	1.5	2	V
		V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =1mA	Q2	1.3	1.6	2.1	V

**Dynamic Characteristics**

Q <sub>g</sub>	Total Gate Charge <sup>3,4</sup>	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =35A	Q1	---	6.5	---	nC	
			Q2	---	22	---		
Q <sub>g</sub>	Total Gate Charge <sup>3,4</sup>	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =35A	Q1	---	11	---		
			Q2	---	45.5	---		
Q <sub>gs</sub>	Gate-Source Charge <sup>3,4</sup>		Q1	---	1.9	---		
			Q2	---	3.2	---		
Q <sub>gd</sub>	Gate-Drain Charge <sup>3,4</sup>		Q1	---	2.6	---		
			Q2	---	6	---		
T <sub>d(on)</sub>	Turn-On Delay Time <sup>3,4</sup>	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =6Ω I <sub>D</sub> =35A	Q1	---	2	---		ns
			Q2	---	4	---		
T <sub>r</sub>	Rise Time <sup>3,4</sup>		Q1	---	3	---		
			Q2	---	6	---		
T <sub>d(off)</sub>	Turn-Off Delay Time <sup>3,4</sup>		Q1	---	5	---		
			Q2	---	12	---		
T <sub>f</sub>	Fall Time <sup>3,4</sup>		Q1	---	5	---		
			Q2	---	18	---		

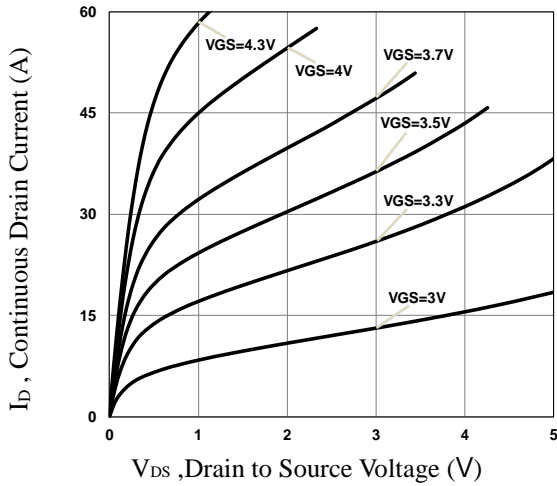
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , F=1MHz	Q1	---	840	---	pF
			Q2	---	2390	---	
C <sub>oss</sub>	Output Capacitance		Q1	---	620	---	
			Q2	---	1050	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		Q1	---	10	---	
			Q2	---	62	---	
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz	Q1	---	1.3	---	Ω
			Q2	---	1	---	Ω

### Drain-Source Diode Characteristics

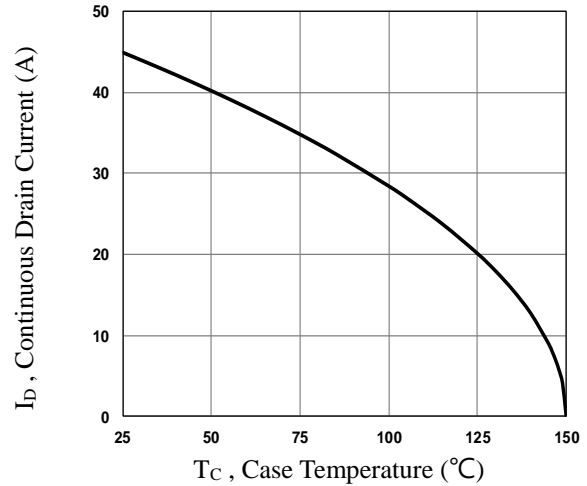
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit		
I <sub>s</sub>	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	Q1	---	---	45	A	
			Q2	---	---	85	A	
I <sub>SM</sub>	Pulsed Source Current <sup>3</sup>		Q1	---	---	90	A	
			Q2	---	---	170	A	
V <sub>SD</sub>	Diode Forward Voltage <sup>3</sup>		V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C	Q1	---	---	1	V
				Q2	---	---	1	V

Note :

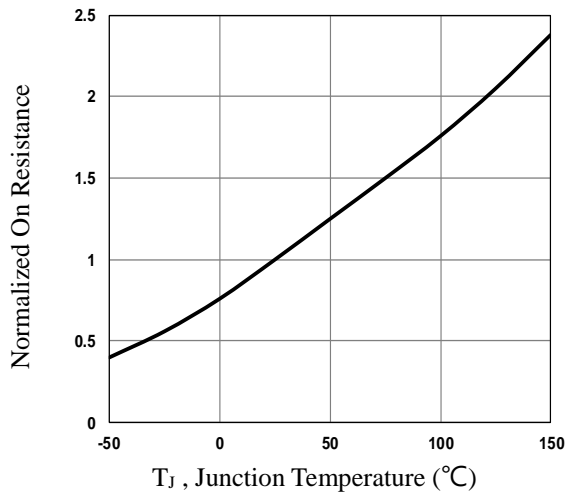
1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, Q1: I<sub>AS</sub>=34.5A, Q2: I<sub>AS</sub>=53A, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C.
3. The data tested by pulsed , pulse width ≤ 300μs , duty cycle ≤ 2%.
4. Essentially independent of operating temperature.



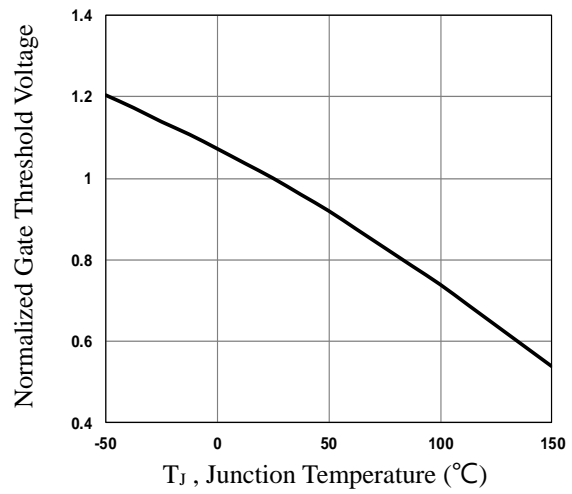
**Fig.1 Q1 Typical Output Characteristics**



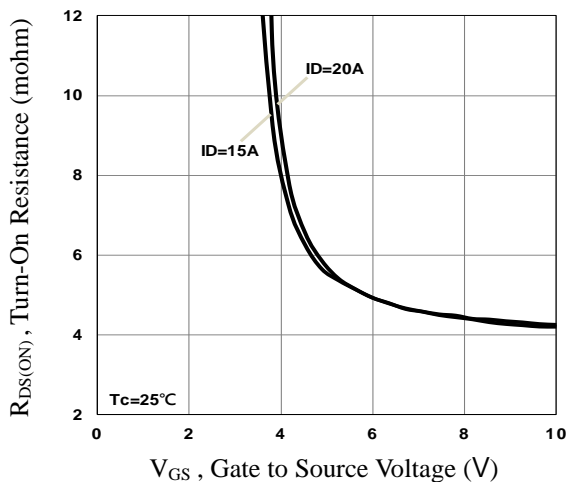
**Fig.2 Q1 Continuous Drain Current vs. T<sub>c</sub>**



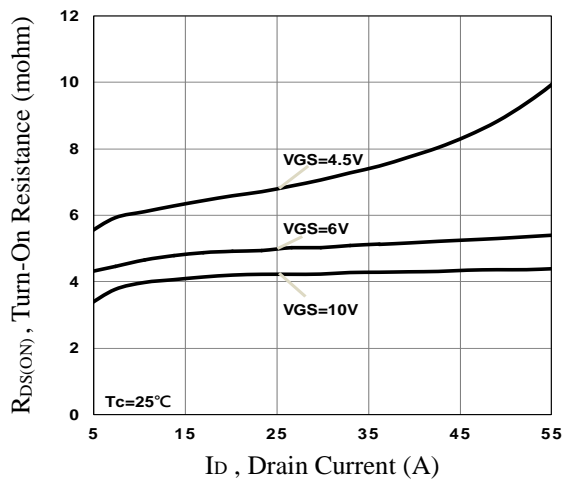
**Fig.3 Q1 Normalized R<sub>DS(on)</sub> vs. T<sub>j</sub>**



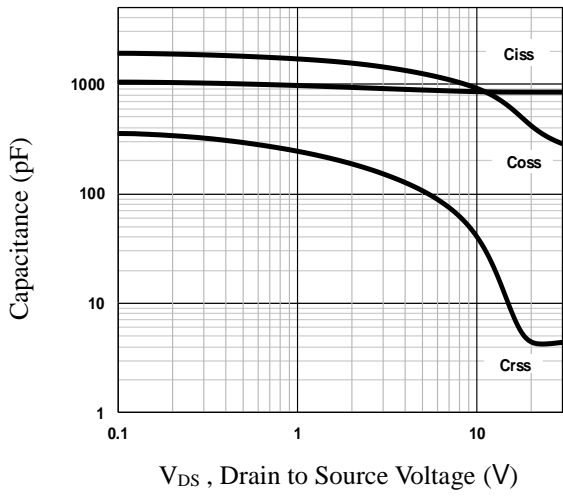
**Fig.4 Q1 Normalized V<sub>th</sub> vs. T<sub>j</sub>**



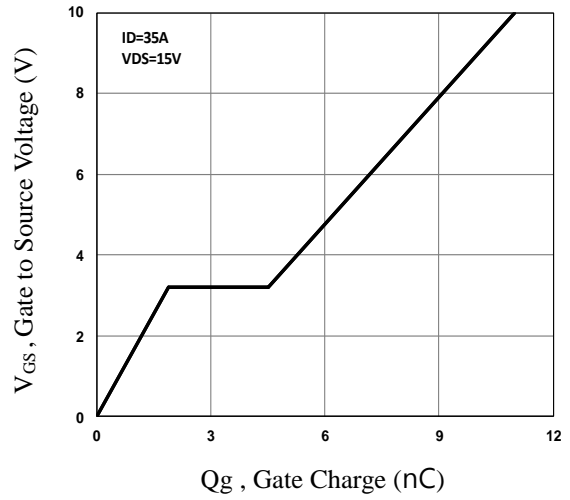
**Fig.5 Q1 Turn-On Resistance vs. V<sub>GS</sub>**



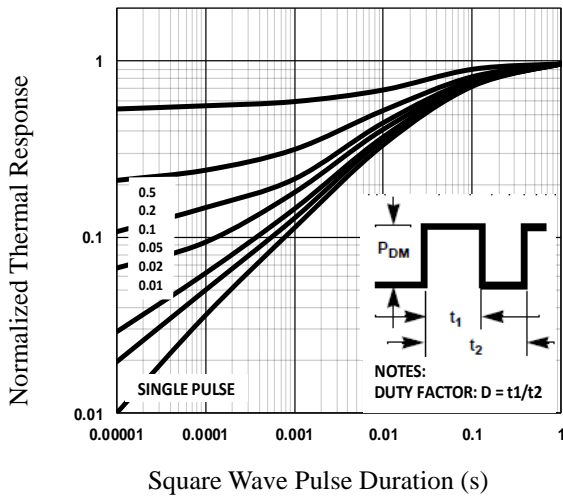
**Fig.6 Q1 Turn-On Resistance vs. I<sub>D</sub>**



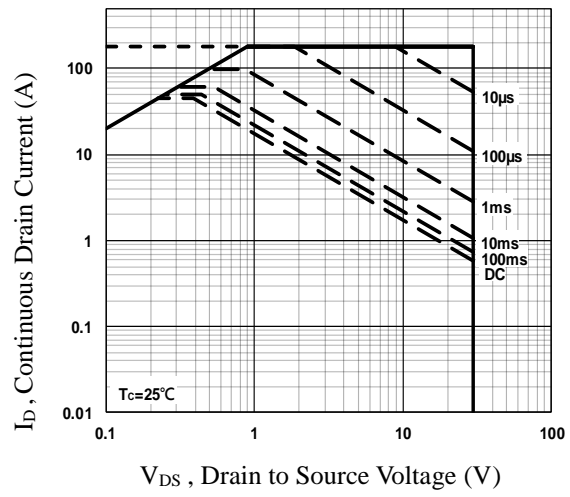
**Fig.7 Q1 Capacitance Characteristics**



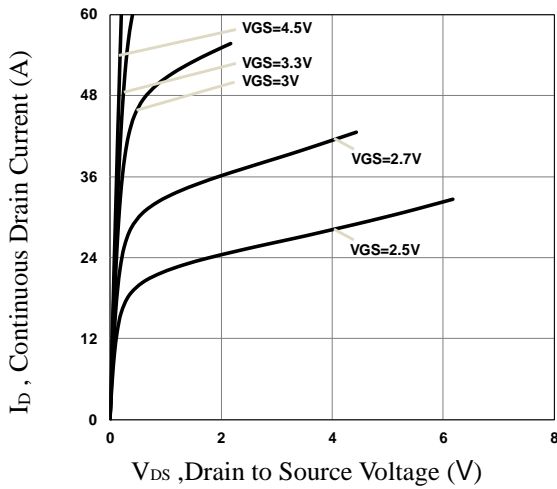
**Fig.8 Q1 Gate Charge Characteristics**



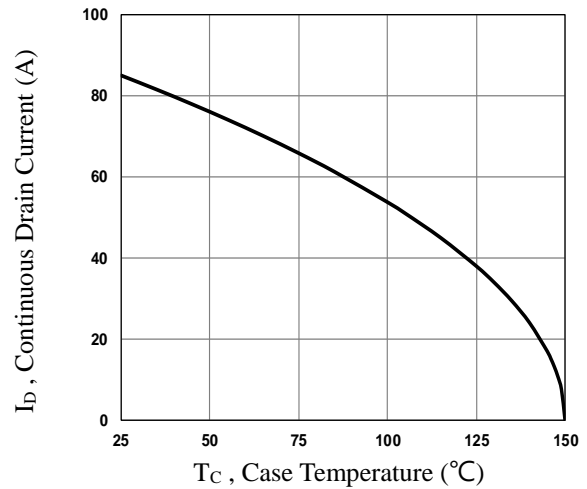
**Fig.9 Q1 Normalized Transient Impedance**



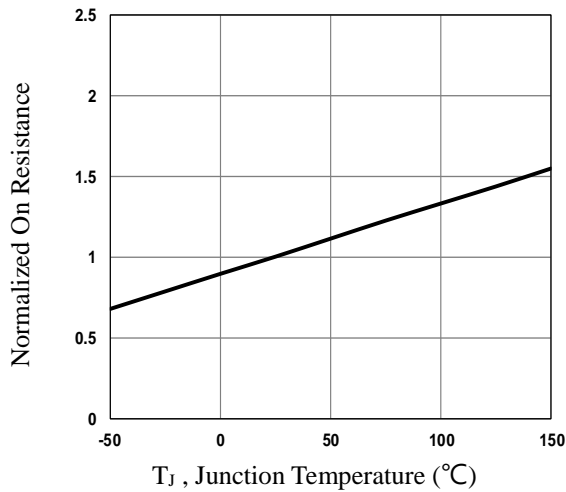
**Fig.10 Q1 Maximum Safe Operation Area**



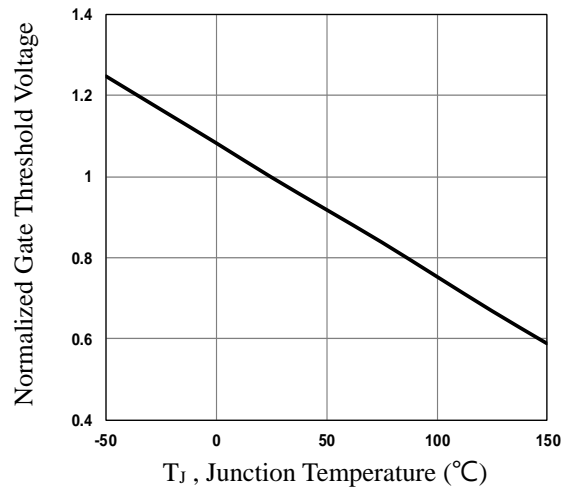
**Fig.11 Q2 Typical Output Characteristics**



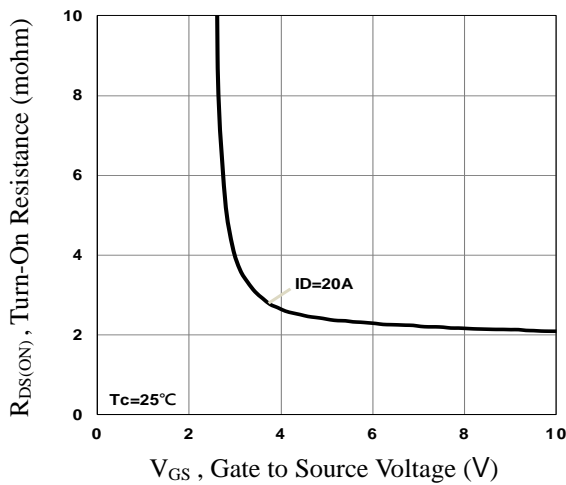
**Fig.12 Q2 Continuous Drain Current vs.  $T_c$**



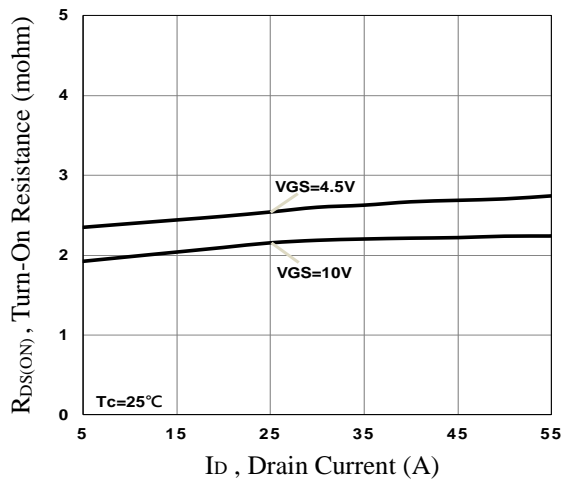
**Fig.13 Q2 Normalized  $R_{DS(ON)}$  vs.  $T_J$**



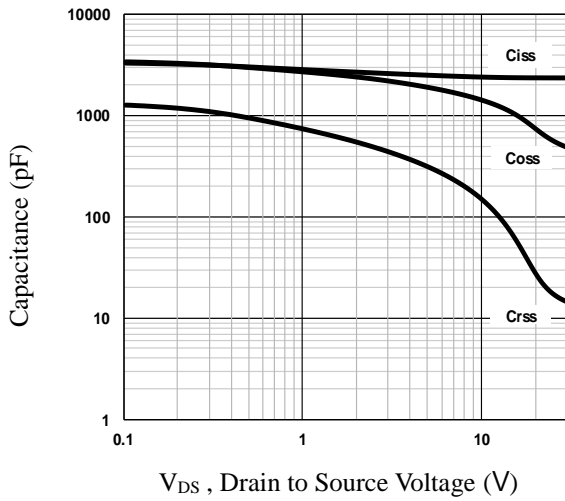
**Fig.14 Q2 Normalized  $V_{th}$  vs.  $T_J$**



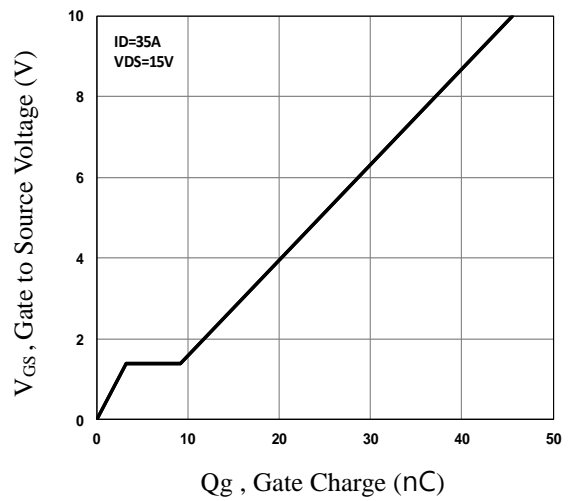
**Fig.15 Q2 Turn-On Resistance vs.  $V_{GS}$**



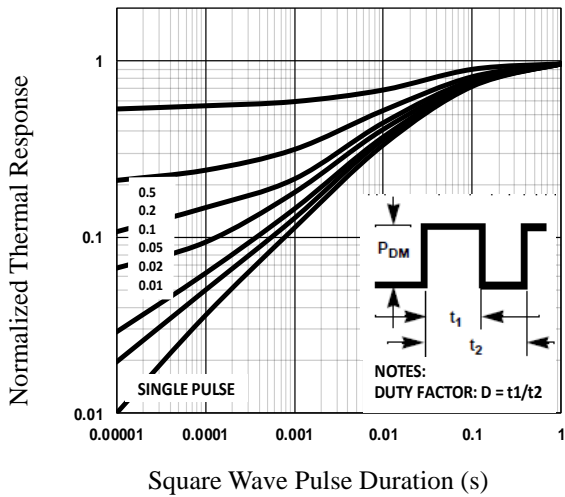
**Fig.16 Q2 Turn-On Resistance vs.  $I_D$**



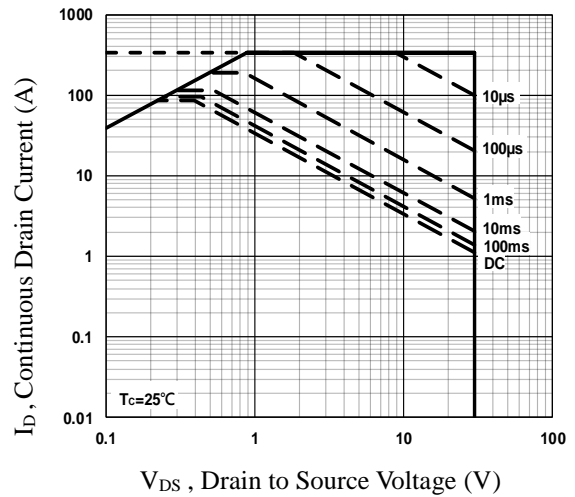
**Fig.17 Q2 Capacitance Characteristics**



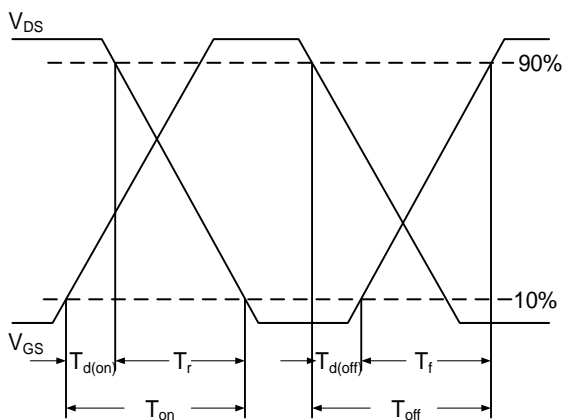
**Fig.18 Q2 Gate Charge Characteristics**



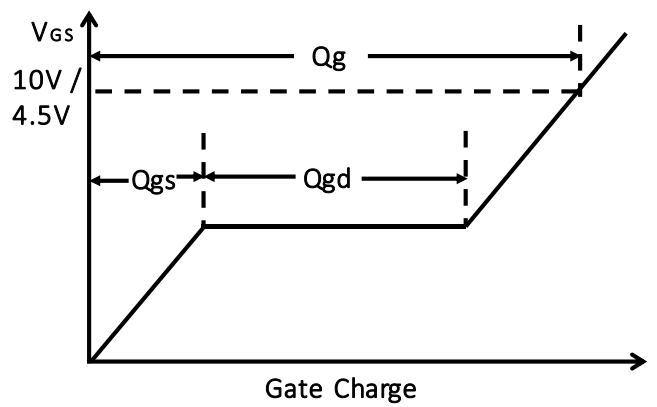
**Fig.19 Q2 Normalized Transient Impedance**



**Fig.20 Q2 Maximum Safe Operation Area**

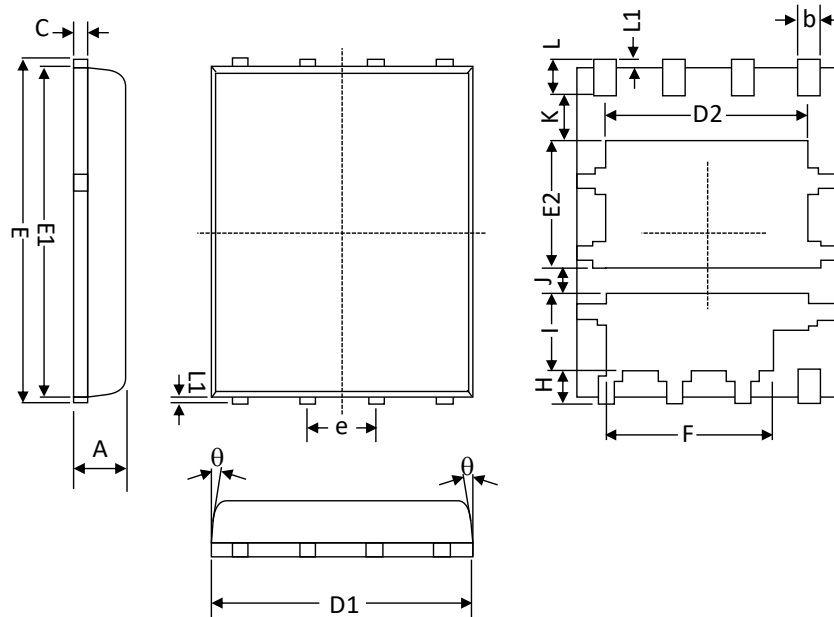


**Fig.21 Switching Time Waveform**



**Fig.22 Gate Charge Waveform**

## PPAK5x6 Asymmetric Dual Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.850	1.100	0.033	0.043
b	0.250	0.510	0.010	0.020
C	0.150	0.300	0.006	0.012
D1	4.800	5.300	0.189	0.209
D2	3.600	3.960	0.142	0.156
E	5.900	6.200	0.232	0.244
E1	5.400	5.850	0.213	0.230
E2	2.000	2.450	0.079	0.096
e	1.270 BSC		0.050 BSC	
F	2.550	3.250	0.100	0.128
H	0.430	0.810	0.017	0.032
I	1.100	1.420	0.043	0.056
J	0.300	0.600	0.012	0.024
K	0.500	-	0.020	-
L	0.350	0.800	0.014	0.031
L1	0.060	0.350	0.002	0.014
θ	0°	14°	0°	14°